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AF ZAW 2133

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kenneth P. Parker

Serial No.: 09/908,948 **Examiner:** Abraham, Esaw T.

Filing Date: July 19, 2001 **Group Art Unit:** 2133

Title: METHOD AND APPARATUS FOR MINIMIZING CURRENT SURGES DURING INTEGRATED CIRCUIT TESTING

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on April 21, 2005

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-1078** the sum of $500.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

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Date of Facsimile:

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Signature:

Respectfully submitted,

Kenneth P. Parker

By

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	09/908,948	Confirmation No. 1925
Appellants	:	Kenneth P. Parker	
Filed	:	July 19, 2001	
TC/A.U.	:	2133	
Examiner	:	Esaw T. Abraham	
Docket No.	:	10001121-1	

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
PO Box 1450
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APPEAL BRIEF

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Board of Patent Appeals and Interferences
United States Patent and Trademark Office
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Alexandria VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated December 21, 2004.

Appellants filed a Notice of Appeal on April 21, 2005.

Real Party in Interest

The real party in interest is Agilent Technologies, Inc., a Delaware corporation headquartered in Palo Alto, California.

Related Appeals and Interferences

There are no related appeals and/or interferences.

Status of Claims

Claims 1-23 remain pending. A copy of the claims is attached as an Appendix to this Appeal Brief.

Status of Amendments

All amendments have been entered.

Although the Advisory Action mailed March 21, 2005 indicates that, "For purposes of Appeal, the proposed amendment(s) will not be entered", appellants are not aware of any un-entered amendments.

Summary of Claimed Subject Matter

In a first embodiment (claim 1), an integrated circuit (e.g., 800, FIG. 8; 1000, FIG. 10; 1100, FIG. 11; 1400, FIG. 14; 1500, FIG. 15) comprises a plurality of interconnected circuit elements (802-812, FIGS. 8, 10 & 11; 1302, FIGS. 14 & 15), and a number of scan chains (see, e.g., scan chain elements 614-626, FIGS. 8, 10 & 11; scan chains 1304-1308, FIGS. 14 & 15) that are interconnected with the plurality of interconnected circuit elements (p. 12, line 16 – p. 14, line 9; p. 16, line 25 – p. 17, line 18). The number of scan chains provide paths through which test data is shifted into and/or out of the integrated circuit. Current surge minimization circuitry (814, 816, FIG. 8; 814, 816, 1002, FIG. 10; 1102, FIG. 11; inputs A1, A2, B1, B2, FIG. 14; 1502-1510, FIG. 15) is interconnected with the plurality of interconnected circuit elements (p. 14, line 10 – p. 16, line 7; p. 17, line 19 – p. 18, line 18). Operation of the current surge minimization circuitry during operation of the number of scan chains minimizes current surges in the integrated circuit.

In a second embodiment (claim 9), an integrated circuit (e.g., 800, FIG. 8; 1000, FIG. 10; 1100, FIG. 11; 1400, FIG. 14; 1500, FIG. 15) comprises a plurality of interconnected circuit elements (802-812, FIGS. 8, 10 & 11; 1302, FIGS. 14 & 15), and a number of scan chains (see, e.g., scan chain elements 614-626, FIGS. 8, 10 & 11; scan chains 1304-1308, FIGS. 14 & 15) that are interconnected with the plurality of interconnected circuit elements (p. 12, line 16 – p. 14, line 9; p. 16, line 25 – p. 17, line 18). The number of scan chains provide paths through which test data is shifted into and/or out of the integrated circuit. The integrated circuit also comprises means (814, 816, FIG. 8; 814, 816, 1002, FIG. 10; 1102, FIG. 11; inputs A1, A2, B1, B2, FIG. 14; 1502-1510, FIG. 15) for minimizing current surges in the integrated circuit as the number of scan chains shift test data into and out of the plurality of interconnected circuit elements (p. 14, line 10 – p. 16, line 7; p. 17, line 19 – p. 18, line 18). In one variation of this embodiment, the means for minimizing current surges comprises means (814, 816, FIG. 8; 814, 816, 1002, FIG. 10; 1102, FIG. 11) for gating out shift induced node state transitions in the integrated circuit as the

number of scan chains shift test data. In another variation of this embodiment, the means for minimizing current surges comprises means (inputs A1, A2, B1, B2, FIG. 14; 1502-1510, FIG. 15) for phasing operation of at least two of the number of shift chains.

In a third embodiment, logic synthesis software (508, FIG. 5; p. 11, line 14 – p. 12, line 12) comprises a number of computer readable media (506, FIG. 5), and computer readable program code stored on the number of computer readable media. The code comprises program code (510, FIG. 5) for reading a circuit description file (502, FIG. 5) that contains data which specifies current surge minimization constraints for a circuit which is described in the circuit description file. At least some of the current surge minimization constraints are defined for operation of the circuit during operation of at least one scan chain of the circuit. The code further comprises 1) rules and design elements (512, FIG. 5) for minimizing current surges in a circuit, and 2) code (514, FIG. 5) for synthesizing current surge minimization circuitry (516, FIG. 5) using the design elements, in conformance with the current surge minimization constraints and the rules for minimizing current surges in a circuit.

In a fourth embodiment, a method (400, FIG. 4; p. 9, line 20 – p. 11, line 13) of designing an integrated circuit (e.g., 800, FIG. 8; 1000, FIG. 10; 1100, FIG. 11; 1400, FIG. 14; 1500, FIG. 15) comprises 1) providing (402, FIG. 4) the integrated circuit with a number of scan chains (see, e.g., scan chain elements 614-626, FIGS. 8, 10 & 11; scan chains 1304-1308, FIGS. 14 & 15) which provide paths through which test data is shifted into and/or out of the integrated circuit, 2) providing (404, FIG. 4) the integrated circuit with current surge minimization circuitry (814, 816, FIG. 8; 814, 816, 1002, FIG. 10; 1102, FIG. 11; inputs A1, A2, B1, B2, FIG. 14; 1502-1510, FIG. 15), and 3) configuring (406-414, FIG. 4) the current surge minimization circuitry to be operated during operation of the number of scan chains.

In a fifth embodiment, a method (1200, FIG. 12; p. 16, lines 8-24) for testing an integrated circuit (e.g., 800, FIG. 8; 1000, FIG. 10; 1100, FIG. 11; 1400, FIG. 14; 1500, FIG. 15) comprises 1) shifting (1202, FIG. 12) test data through a number of

scan chains (see, e.g., scan chain elements 614-626, FIGS. 8, 10 & 11; scan chains 1304-1308, FIGS. 14 & 15) of the integrated circuit, and 2) during at least a portion of the shifting, applying (1204, FIG. 12) current surge minimization signals to the integrated circuit.

In a sixth embodiment, a method (1600, FIG. 16; p. 18, line 19 – p. 19, line 3) for testing an integrated circuit (1400, FIG. 14; 1500, FIG. 15) comprises 1) providing (1602, FIG. 16) test data to at least two scan chains (1304-1308, FIGS. 14 & 15) of the integrated circuit, and 2) shifting (1604, FIG. 16) test data through the at least two scan chains in parallel, but out-of-phase, while at least a portion of the test data is being provided to the at least two scan chains.

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 1-20 should be rejected under 35 USC 103(a) as being unpatentable over Wagner et al. (US 6,389,566).

2. Whether claims 21-23 should be rejected under 35 USC 103(a) as being unpatentable over Wu (US 5,831,992).

Argument

1. Claims 1-20 should not be rejected under 35 USC 103(a) as being unpatentable over Wagner et al. (US 6,389,566; hereinafter "Wagner").

A. Claim 1

Appellant's claim 1 recites:

1. An integrated circuit, comprising:
   a) a plurality of interconnected circuit elements;
   b) a number of scan chains which are interconnected with the plurality of interconnected circuit elements, said number of scan chains providing paths through which test data is shifted into and/or out of the integrated circuit; and
   c) current surge minimization circuitry which is interconnected with said plurality of interconnected circuit elements, whereby operation of said current surge minimization circuitry during operation of said number of scan chains minimizes current surges in said integrated circuit.

In rejecting appellant's claim 1, the Examiner asserts that Wagner teaches a serial scan chain, but does not explicitly teach "current surge minimization circuitry which is interconnected with [a] plurality of interconnected circuit elements, whereby operation of said current surge minimization circuitry during operation of [a] number of scan chains minimizes current surges in [an] integrated circuit." See, e.g., 12/21/2004 Final Office Action, sec. 1, p. 4. Appellant agrees with the Examiner on this point.

The Examiner also asserts that Wagner teaches:

> . . .scan shift race conditions are minimized by providing a weak scan output signal driver and inserting delay elements within a cell for a scan flip-flop in the scan signal path (abstract, col. 3, lines 39-58) and further Wagner et al. teach a preceding equation for avoiding race conditions during scan shift operations (see col. 6, lines 15-30) including applying the functionality of CMOS device ***(In CMOS technology, both kinds of transistors (N-type transistors) or (P-type transistors) are used in a complementary way to form a current gate that forms an effective means of electrical control and as the current direction changes***

> ***more rapidly, however, the transistors become hot. This characteristic tends to limit the speed at which microprocessors can operate)*** for minimizing the race ***(surge)*** current ***(see col. 6, lines 31-45)*** which Wagner's system is basically teaching the same system and method as the applicant's claim to minimize current.
>
> 12/21/2004 Final Office Action, sec. 1, pp. 4-5 (emphasis added).

Appellant respectfully disagrees. The Examiner seems to suggest, although perhaps inadvertently, that the emphasized portions of his assertions are taught or suggested by Wagner in col. 6, lines 31-45. This is absolutely not the case. In fact, Wagner's disclosure is devoid of any discussion of "transistors becoming hot" or currents "surging". Rather, Wagner's race mitigation techniques are designed to prevent "an incorrect test vector being loaded into the scan chain or an inaccurate reading of the system state being provided." See Wagner, col. 3, lines 13-14.

Although the Examiner suggests that one of ordinary skill in the art would think to modify Wagner's teachings for the purpose of minimizing current surges during scan chain operation, appellant does not believe this to be the case. Of note, Wagner discloses the incorporation of delay elements in the path along which test data is shifted (i.e., from S_{IN} to S_{OUT}; see, e.g., Wagner's FIG. 2). Although Wagner's delay elements might help to mitigate *race conditions* in the scan chain's data path, appellant fails to see how Wagner's delay elements would minimize *current surges*. The addition of more active transistors *in the scan chain's path* would seem to only increase the current draw of the scan chain (tending not to minimize current surges).

In response to appellant's above remarks, the Examiner asserted that Wagner's use of a weak signal driver and delay elements to drive data through a scan chain necessitates the conclusion that:

> . . .there is no difference between the applicant's minimizing a sudden current rise or surge (which the goal is to minimize a current error) and the minimization of scan shift race conditions in the prior art since the both the applicant's

> invention and Wagner's system minimizes current errors (current rises or races).
>
> 12/21/2004 Final Office Action, p. 2.

Appellant believes the Examiner inappropriately equates the concepts of "race" and "surge". According to one source, a current "surge" is a sudden and possibly damaging increase in current; and a "race" is a condition in which data propagates rapidly through a logic circuit, far ahead of the clock signal intended to control its passage. A current surge does not necessarily lead to a "race" or "error". On the other hand, a race does not necessarily lead to a "current surge". Wagner's disclosure is void of any discussion of current surges (or the mitigation thereof).

For the above reasons, appellant believes the Examiner's rejection of his claim 1 is not supported and should be withdrawn. Appellant's claims 2-8 are believed to be allowable at least for the reason that they depend from claim 1. However, appellant's claims 2-8 are also believed to be allowable for other reasons, as discussed in sections B – F of this Argument, below.

B. Claim 2

With respect to appellant's claim 2, the Examiner discusses how Wagner teaches how to avoid race conditions "by increasing the signal transition time of a flip-flop during a shift operation" and by using a weak signal driver that has low current drive capability. See, 12/21/2004 Final Office Action, sec. 1, p. 5. However, appellant fails to see the relation of this teaching to his claim. His claim discloses the use of "transistors receiv[ing] a number of gating signals during operation of [a] number of scan chains, which number of gating signals disable current flow through the ones of said plurality of interconnected circuit elements." Although Wagner does disclose the use of gating signals, Wagner's gating signals are "within" a scan chain, and they do not readily appear to mitigate current surges in "circuit elements" that

are "interconnected with" a "number of scan chains". Appellant therefore believes that claim 2 is additionally allowable over Wagner's teachings.

C. Claim 3

With respect to appellant's claim 3, the Examiner does not disclose where Wagner teaches "an electrical network connecting gates of the number of [gated] transistors to one or more external inputs of the integrated circuit". Appellant believes that Wagner is devoid of any such disclosure, and claim 3 is therefore additionally allowable over Wagner's teachings.

D. Claim 4

With respect to appellant's claim 4, the Examiner does not disclose where Wagner teaches "a number of delay elements which cause a signal applied to one of said external inputs to be applied to the gates of various of said number of [gated] transistors at different times". Appellant believes that Wagner is devoid of any such disclosure, and claim 4 is therefore additionally allowable over Wagner's teachings.

E. Claim 5

With respect to appellant's claim 5, the Examiner does not disclose where Wagner teaches "a number of logic elements which cause at least one of said number of gating signals to change state in response to data shifted through at least one of said number of scan chains". Appellant believes that Wagner is devoid of any such disclosure, and claim 5 is therefore additionally allowable over Wagner's teachings.

F. Claims 6-8

With respect to appellant's claim 6, the Examiner asserts that Wagner teaches the elements of this claim in col. 1, last paragraph. However, this paragraph does not teach "at least first and second scan chains" or "external shift signal inputs corresponding to the first and second scan chains". In fact, appellant cannot find such teachings anywhere in Wagner's disclosure.

The Examiner further asserts that Wagner teaches first and second scan chains, because:

> . . .Wagner in figure 1 teach scan flip-flops 15A-G are formed into a serial scan chain, i.e., a serial shift register, by connecting the Q data output of one scan flip-flop to the S_{IN} port of another scan flip-flop.

12/21/2004 Final Office Action, p. 3.

Appellant disagrees and believes the figure referred to by the Examiner is clearly supportive of the fact that Wagner only discloses a *single* scan chain.

As with claim 6, appellant's claim 7 recites "first and second scan chains", which feature does not appear to be taught anywhere in Wagner's disclosure.

Appellant therefore believes that claims 6-8 are additionally allowable over Wagner's teachings.

G. Claims 9-11

Appellant's claims 9-11 are believed to be allowable at least for reasons similar to why appellant's claim 1 is believed to be allowable. Appellant's claim 11 is also believed to be allowable in that Wagner does not teach "means for phasing operation of" at least two scan chains. Although the Examiner asserted that such phased operation is commonly known to those of ordinary skill in the art, appellant disagreed, and the Examiner did not provide any reference to support his assertion.

Furthermore, the phasing of scan chain operation first requires the existence of two scan chains. As already argued by appellant in section F of this Argument, Wagner fails to disclose the existence or use of two scan chains.

Appellant notes that, on page 6 of the 12/21/2004 Final Office Action, the Examiner asserts that, "performing a phase operation is required in most of scan testing systems since the operation commonly deals with different shifting signals (test data) between scan chains." Appellant believes the Examiner is mingling concepts here. Although it is common to shift test data through a scan chain, or between the "elements" of a scan chain, it is not common to shift test data "between scan chains". Furthermore, although it is known that a *single* scan chain may be operated in response to a combination of out-of-phase shift signals, appellant is unaware of *different* scan chains being operated out-of-phase so as to minimize current surges in the device in which the scan chains are implemented.

H. Claims 12 & 13

Appellant's claims 12 and 13 are believed to be allowable at least for reasons similar to why appellant's claim 1 is believed to be allowable. In addition, these claims are believed to be allowable because Wagner fails to disclose *any* sort of "logic synthesis software" – and especially software that includes "code for synthesizing current surge minimization circuitry using. . .design elements [for minimizing current surges in a circuit], in conformance with. . .current surge minimization constraints [provided in a circuit description file] and. . .rules for minimizing current surges in a circuit", as recited in appellant's claim 12.

I. Claims 14-17

Appellant's claim 14 is believed to be allowable at least for reasons similar to why appellant's claim 1 is believed to be allowable.

Appellant's claim 15 is believed to be additionally allowable over claim 14 in that, as previously argued, Wagner fails to disclose the existence or use of two scan chains. As a result, Wagner certainly cannot disclose how to operate two or more scan chains to minimize current surges (i.e., by providing an integrated circuit with "distinct external inputs for receiving shift signals corresponding to two different ones of said. . .scan chains).

Appellant's claim 16 is believed to be additionally allowable over claim 14 in that Wagner's failure to disclose two scan chains makes it impossible for Wagner to disclose out-of-phase operation of two scan chains.

J. Claims 18-20

Appellant's claims 18-20 are believed to be allowable at least for reasons similar to why appellant's claim 1 and other claims are believed to be allowable.

2. Claims 21-23 should not be rejected under 35 USC 103(a) as being unpatentable over Wu (US 5,831,992).

A. Claim 21

Appellant's claim 21 recites:

21. A method of testing an integrated circuit, comprising:
a) providing test data to at least two scan chains of the integrated circuit; and
b) shifting test data through the at least two scan chains in parallel, but out-of-phase, while at least a portion of the test data is being provided to the at least two scan chains.b) means for programming the client to display the measurement data three-dimensionally, and in real-time.

In rejecting appellant's claims 21-23, the Examiner cites a reference (Wu) that discloses the use of two scan chains. The Examiner then admits that the remaining limitations of appellant's claims (e.g., out-of-phase operation of the two scan chains) are not actually taught by Wu. However, the Examiner asserts that these missing limitations would be obvious to one of ordinary skill in the art. Appellant disagreed, and the Examiner did not provide any reference to support his assertion.

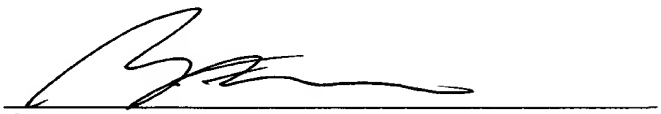
Appellant notes that, although Wu discloses the use of a plurality of scan chains, Wu's disclosure focuses on an "analytical fault diagnostic methodology" and, more specifically, on how data shifted out of a plurality of scan chains is compacted and then interpreted. Appellant cannot find any teaching regarding how Wu operates his plural scan chains. As a result, appellant can only assume that Wu's scan chains are operated in parallel and in-phase, in a conventional manner.

Appellant believes his claims 21-23 are allowable over Wu's teachings for at least the above reasons.

3. Conclusion

In light of the above arguments, Appellants request the allowance of their pending claims.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.

By: 

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Claims Appendix

Claim 1: An integrated circuit, comprising:

a) a plurality of interconnected circuit elements;

b) a number of scan chains which are interconnected with the plurality of interconnected circuit elements, said number of scan chains providing paths through which test data is shifted into and/or out of the integrated circuit; and

c) current surge minimization circuitry which is interconnected with said plurality of interconnected circuit elements, whereby operation of said current surge minimization circuitry during operation of said number of scan chains minimizes current surges in said integrated circuit.

Claim 2: An integrated circuit as in claim 1, wherein:

a) said current surge minimization circuitry comprises a number of transistors which are coupled to ones of said plurality of interconnected circuit elements; and

b) said number of transistors receive a number of gating signals during operation of said number of scan chains, which number of gating signals disable current flow through the ones of said plurality of interconnected circuit elements.

Claim 3: An integrated circuit as in claim 2, wherein the current surge minimization circuitry comprises an electrical network connecting gates of the number of transistors to one or more external inputs of the integrated circuit, wherein the number of gating signals is applied to the number of transistors via application of one or more signals to said one or more external inputs.

Claim 4: An integrated circuit as in claim 3, wherein the electrical network comprises a number of delay elements which cause a signal applied to one of said external inputs to be applied to the gates of various of said number of transistors at different times.

Claim 5: An integrated circuit as in claim 3, wherein the electrical network comprises

a number of logic elements which cause at least one of said number of gating signals to change state in response to data shifted through at least one of said number of scan chains.

Claim 6: An integrated circuit as in claim 1, wherein:

a) the number of scan chains comprises at least first and second scan chains; and

b) the current surge minimization circuitry comprises distinct, external shift signal inputs corresponding to the first and second scan chains.

Claim 7: An integrated circuit as in claim 1, wherein:

a) the number of scan chains comprises at least first and second scan chains; and

b) the current surge minimization circuitry comprises a shift signal generator comprising a number of delay elements for delaying generation of a second shift signal with respect to generation of a first shift signal, said first shift signal being provided to a shift signal input of said first scan chain, and said second shift signal being provided to a shift signal input of said second scan chain.

Claim 8: An integrated circuit as in claim 7, wherein only one external input of said integrated circuit is coupled to a shift signal input of said shift signal generator.

Claim 9: An integrated circuit, comprising:

a) a plurality of interconnected circuit elements;

b) a number of scan chains which are interconnected with the plurality of interconnected circuit elements, said number of scan chains providing paths through which test data is shifted into and/or out of the integrated circuit; and

c) means for minimizing current surges in said integrated circuit as said number of scan chains shift test data into and out of said plurality of interconnected circuit element.

Claim 10: An integrated circuit as in claim 9, wherein said means for minimizing current surges comprises means for gating out shift induced node state transitions in said integrated circuit as said number of scan chains shift test data.

Claim 11: An integrated circuit as in claim 9, wherein said means for minimizing current surges comprises means for phasing operation of at least two of said number of shift chains.

Claim 12: Logic synthesis software, comprising:

a) a number of computer readable media; and

b) computer readable program code stored on the number of computer readable media, the computer readable program code comprising:

i) program code for reading a circuit description file, the circuit description file comprising data which specifies current surge minimization constraints for a circuit which is described in the circuit description file, at least some of said current surge minimization constraints being defined for operation of the circuit during operation of at least one scan chain of the circuit;

ii) rules and design elements for minimizing current surges in a circuit; and

iii) program code for synthesizing current surge minimization circuitry using said design elements, in conformance with said current surge minimization constraints and said rules for minimizing current surges in a circuit.

Claim 13: Logic synthesis software as in claim 12, wherein the computer readable program code further comprises program code for synthesizing said circuit.

Claim 14: A method of designing an integrated circuit, comprising:

a) providing the integrated circuit with a number of scan chains which provide paths through which test data is shifted into and/or out of the integrated circuit; and

b) providing the integrated circuit with current surge minimization circuitry,

and configuring said current surge minimization circuitry to be operated during operation of said number of scan chains.

Claim 15: A method as in claim 14, wherein said number of scan chains is at least two, and wherein providing the integrated circuit with current surge minimization circuitry comprises providing the integrated circuit with distinct external inputs for receiving shift signals corresponding to two different ones of said number of scan chains.

Claim 16: A method as in claim 14, wherein providing the integrated circuit with current surge minimization circuitry comprises providing the integrated circuit with a shift signal generator, said shift signal generator generating at least a first shift signal which i) is provided to a first of the number of scan chains, and ii) is out-of-phase with at least a second shift signal which is provided to a second of the number of scan chains.

Claim 17: A method as in claim 14, wherein providing the integrated circuit with current surge minimization circuitry comprises:

a) routing a number of gating signal lines to a number of circuit elements of the integrated circuit; and

b) routing each of said gating signal lines to an external input of the integrated circuit.

Claim 18: A method of testing an integrated circuit, comprising:

a) shifting test data through a number of scan chains of the integrated circuit; and

b) during at least a portion of said shifting, applying current surge minimization signals to the integrated circuit.

Claim 19: A method as in claim 18, wherein applying current surge minimization signals to the integrated circuit comprises applying gating signals to circuit elements

of the integrated circuit.

Claim 20: A method as in claim 18, wherein applying current surge minimization signals comprises changing the state of at least one current surge minimization signal while said at least one current surge minimization signal is being applied.

Claim 21: A method of testing an integrated circuit, comprising:

a) providing test data to at least two scan chains of the integrated circuit; and

b) shifting test data through the at least two scan chains in parallel, but out-of-phase, while at least a portion of the test data is being provided to the at least two scan chains.

Claim 22: A method as in claim 21, wherein operating the at least two scan chains comprises:

a) providing at least a first shift signal to a first, but not a second, of the at least two scan chains; and

b) providing at least a second shift signal to the second, but not the first, of the at least two scan chains;

wherein the second shift signal is out-of-phase with the first shift signal.

Claim 23: A method as in claim 21, wherein operating the at least two scan chains comprises:

a) providing at least a first shift signal to a first of the at least two scan chains; and

b) providing at least a second shift signal to a second of the at least two scan chains;

wherein the first shift signal, the second shift signal, and any other shift signal provided to the first and second scan chains, are out-of-phase with respect to one another.

Evidence Appendix

None.

Related Proceedings Appendix

None.